

DESIGN EXERCISE 1

Date: 1st February 2012Due: 15th February 2012

[Transistor Models: T15D Level 3 (Supplied)]

1. Inverting Amplifiers

Using a combination of analytic calculations and HSpice, obtain the transfer characteristics for an NMOS inverting amplifier with the following loads for the input transistor:

- a) 50k Ω resistor
- b) NMOS enhancement
- c) PMOS enhancement
- d) PMOS active current source

Compare these results with those obtained from:

- e) A CMOS inverting amplifier
- f) A double cascode stage (NMOS cascode input with a PMOS cascode load)

Design your amplifiers to produce the most symmetric transfer characteristic possible. Use an aspect ratio of 6/1.2 for the NMOS input transistor in the inverting amplifiers in parts (a) through (d): assume that the process requirements dictate that the transistor dimensions must be in integer multiples of 0.3 μm i.e. a width of 9.9 μm is acceptable; a width of 10.0 μm is not. Using HSpice, obtain values for the small signal input and output resistance and the voltage gain at the appropriate operating point. Use rail voltages of $V_{DD} = 4\text{V}$ and $V_{SS} = 0\text{V}$ with $K'_N = 126\mu\text{A}\cdot\text{V}^{-2}$ and $K'_P = 40\mu\text{A}\cdot\text{V}^{-2}$; for all other parameters use those for the default Level 3 transistor models. Make sure that you use the same model for all transistors of the same type. For parts (e) and (f), you may alter the aspect ratio of the NMOS input transistor.

2. Loads

Add a load, comprising a 10k Ω resistor in parallel with a 1pF capacitor, to each amplifier. Connect the load to the output through a coupling capacitor of 2 μF . Using the results from the previous question, bias the input of each amplifier for maximum gain and plot the gain (in dB) as a function of frequency over a range sufficient to show clearly the low and high frequency 3dB points.

Write a short report for each amplifier as detailed in the attachment.