

DESIGN EXERCISE 2

Date: 5th March 2004

Due: See Individual Questions

[Transistor Models: http://www.ee.cooper.edu/ice/labresources/t3cs_level3.inc][Transistor Models: http://www.ee.cooper.edu/ice/labresources/ami_models/]

1. CMOS Amplifier I

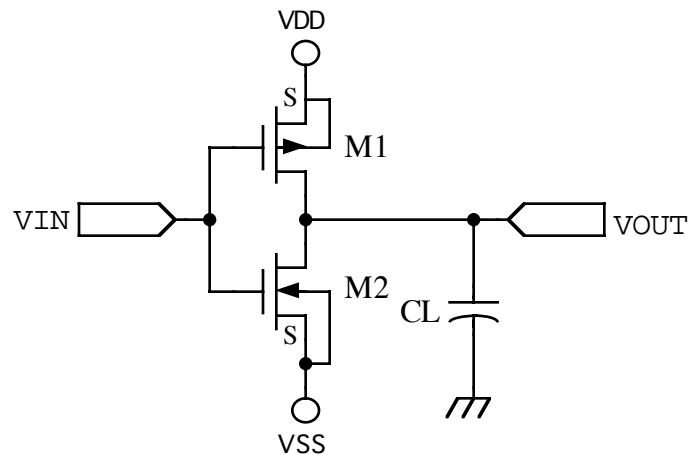
(Design/Simulation: 3/25/04 Layout: 4/1/04)

Design an amplifier based on the CMOS inverter shown below. Commence with a *hand* design using the Level 3 models (t3cs_level3.inc), then use HSpice to verify your result with the Level 49 (BSIM3v3) models (Proprietary AMI Models). What do you think are the principal contributions to the differences between your hand calculation and those from the simulation?

Optimize your design with HSpice and the Level 49 models. Draw the schematic with **Composer-Schematic**, extract the netlist and simulate it within **Analog Environment**: the results should be *identical* to those from your earlier simulation. Next, lay out the circuit with **Virtuoso** and check that the layout does not violate any of the design rules using DRC. Finally, extract the circuit, perform a LVS check and simulate your extracted netlist in **Analog Environment**. Do you observe any changes? **Note:** Do **not** include the load capacitor in your layout or schematic. This must be added separately to the netlist.

The amplifier must have a symmetric output swing with the following characteristics:

Gain: >25dB

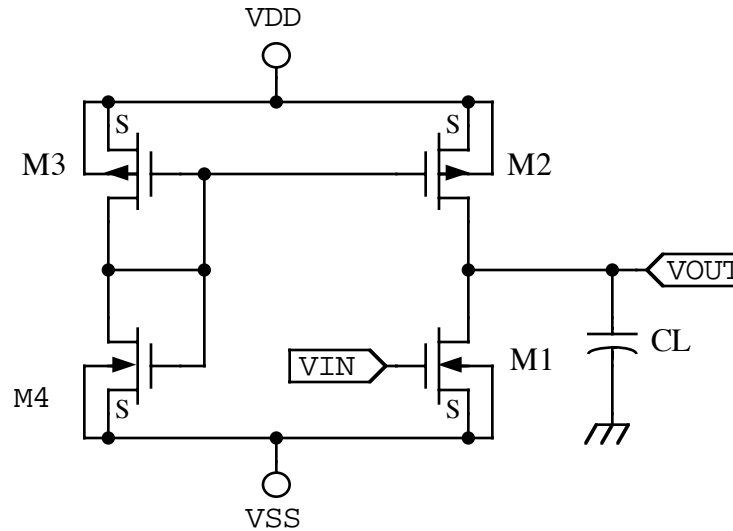
 V_{DD} 5 V V_{SS} 0VSR 10 V. μ s⁻¹ C_L 10 pF

Estimate the upper 3dB frequency and GBW product and compare them with the results you obtained from the simulation using your final layout. Why is this type of amplifier not suitable for resistive loads?

2. CMOS Amplifier II

(Design/Simulation: 3/25/04 Layout: 4/1/04)

One of the fundamental aspects of integrated circuit design is good layout. The object of this exercise is to introduce you to some aspects of layout that are crucial to obtaining circuits whose actual characteristics correspond to those of the simulation.



In the circuit above, the PMOS “load” transistor from the CMOS amplifier has been replaced by an active current source, M2.

Following the procedure outlined in the previous question, design an amplifier with the above topography whose characteristics are as close as possible to those of the CMOS amplifier in the previous question. Using $V_{DD} = 5V$ and $V_{SS} = 0V$, set the current through the biasing circuit, M3 and M4, to that required for the inverting amplifier.

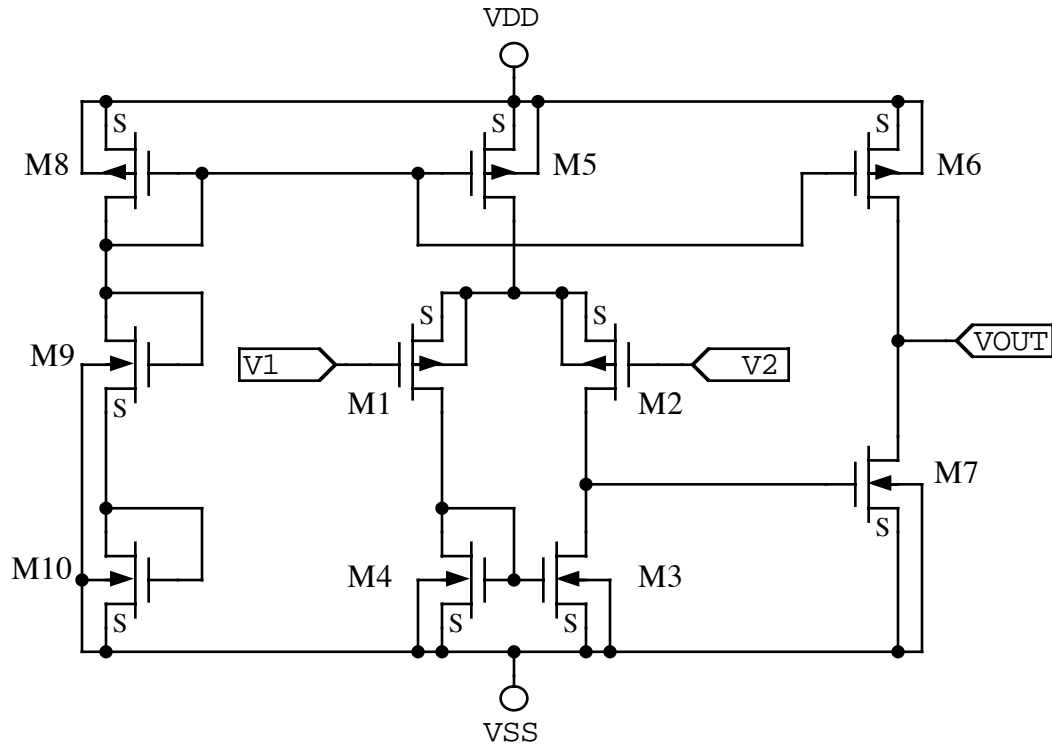
Lay the circuit out within a rectangular boundary so that it occupies the minimum possible area: when arranging your components, remember that the mirror transistors should be as identical as possible and as close as possible. Ideally, the surface within the enclosing boundary will contain the minimum amount of vacant space.

Estimate the upper 3dB frequency and GBW product and compare them with the results you obtained from the simulation using your final layout.

3. Operational Amplifier

(Design/Simulation: 4/1/04 Layout: 4/1/04)

One of the fundamental building blocks of analog and mixed signal circuits is the operational amplifier; an example of which is reproduced below.



Design an operational transconductance amplifier for which the differential stage has a gain of approximately 48dB for a bias current of $2.5 \mu\text{A}$ with $V_{DD} = 5\text{V}$ and $V_{SS} = 0\text{V}$. Set the bias current through the output stage for a gain of about 26 dB and a slew rate of about $2 \text{ V}\cdot\mu\text{s}^{-1}$ with a load capacitance of 5pF .

To minimize the offset voltage for the differential pair, it is vital that transistors M1 and M2 are laid out with a common centroid geometry. There are other important considerations for circuit layout that we will cover in class. Commence with the differential pair and finish with the bias stage.

When you reach the layout/extract phase of your design, monitor the common mode gain, the CMRR, the PSRR and the frequency response as you alter your circuit layout.

T. J. Cumberbatch

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