

DESIGN EXERCISE 4

Phase-Locked Loops Report

Due: 5PM EST 6th May 2011

1. Paper Submission:

Report:

Discuss **your** approach to the overall design, **your** compromises, the thinking behind **your** layout, and the simulated behavior of **your** complete PLL. Talk about the aspects of this project that made **you** think about design and implementation - do *not* reproduce large tracts of *standard* theory or *standard* explanation.

Include data which describe the overall behavior of your circuit such as: the linearity of the gain for your VCO, the static phase error, the width of your dead zone, values of natural frequency, damping factor, the poles and zeros of the circuit, and any other parameters you deem pertinent. Take care with this report - it is **the most important document** for this course. **[Six pages text minimum]**

Schematic Diagrams:

Make these **legible** - use the NCSU facility for publication quality schematics (black on white). Each transistor should be annotated with the name used in your write-up and its dimensions in the form W:L. Suppress the printing of net names and any other spurious information.

- i) An overall schematic for the complete PLL.
- ii) PFD
- iii) Each type of logic gate
- iv) VCO
- v) Charge Pump and Low Pass Filter

Plots

- i) Gain curve of VCO from 80MHz to 120MHz.
- ii) V_{control} (VCO control voltage) as a function of time from startup until frequency and phase lock at 100MHz.
- iii) Composite Plot (4 SEPARATE plots on the same page) - details of the following voltages as a function of time when the PLL is frequency and phase-locked at 100MHz:
 - a) V_{ref}
 - b) V_{control}
 - c) V_{vco} (VCO output voltage)
 - d) V_{up} (Up signal from PFD)
 - e) V_{down} (Down Signal from PFD)

iv) V_{control} as a function of time during the switchover from a reference frequency of 100MHz to a frequency of 111.111MHz (90ns period) - your time window should be large enough to cover the interval covering phase and frequency lock at 100MHz to the same at 111.111MHz

v) Spectral content of VCO output in the frequency range 90 - 110MHz when the PLL is phase and frequency locked at 100MHz.

2. Electronic Submission:

Complete Project Library:

All the files associated with your PLL must be in their own directory inside your group directory so that I can run LVS, DRC and simulations. Each of you must ensure that a copy of your cadence library file (**cds.lib**) is in the top level of your group directory.

The component parts of your ADC must be labeled as follows:

Group code_PLxx (e.g. XX_PLxx) where xx refers to the subcircuit

XX_PLPFD is the phase-frequency detector

XX_PLVCO is the voltage controlled oscillator

XX_PLCPF is the low pass filter and charge pump

and so on - PLEASE do not use more than a three letter extension code.

Submissions that DO NOT adhere to this format will not be accepted - for example bf-ADCmp is NOT ACCEPTABLE neither is xy-mainelobster.yuk and so on.

Email Complete Extracted Net List (as a separate file): (with all commands used to simulate your circuit) as Group code_PLL.SP (e.g. XX_PLL.SP) PLUS any INCLUDED files.

Email Layouts of VCO, PFD and complete PLL as .gif Images:

Name your images XX_PLVCO.gif, XX_PLPFD.gif, XX_PLL.gif respectively. Follow exactly the same procedure you used for the operational amplifiers.

You will receive a full color plot of your PLL layout next semester - should you wish. The best designs will be framed and hung on the walls of the ICE laboratory and elsewhere.

*If you cannot make it by the given date - you MUST let me know. I am sure that we can come to an arrangement if you have a valid reason - **MISSING the deadline with NO explanation will result in an F for the course.***

3. MOSIS Submission: (www.mosis.org)

All designs MUST be DRC and LVS clean. You will not be allowed to tape out until they are.

N.B. All submissions will be very thoroughly checked inside and outside the padframe.

NO ONE MAY SUBMIT A DESIGN TO MOSIS WITHOUT MY PRIOR APPROVAL.

You will not graduate from Cooper Union until you have filed a report on the behavior of your integrated circuit with MOSIS!

T. J. Cumberbatch
1.11 2/4/12